The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A method of operating a cryptographic data processing system that comprises a host processor, a system memory coupled to the host processor, and a cryptographic processor integrated circuit that comprises a local memory and is coupled to the host processor and the system memory, the method comprising:

loading at least one operand from the system memory to the local memory; and

executing an instruction using the cryptographic processor that references the at least one operand using a first relative position in the local memory, comprising:

generating a result based on the at least one operand; and

storing the result at a second relative position in the local memory;

wherein the first relative position comprises a first offset from a base address in the local memory, and the second relative position comprises a second offset from the base address in the local memory; and

wherein the local memory is exclusively associated with the cryptographic processor.

2. (Original) The method of Claim 1, wherein loading at least one operand from the system memory to the local memory comprises loading at least two operands from the system memory to the local memory, and executing the instruction comprises:

executing the instruction using the cryptographic processor that references a first one of the operands using the first relative position in the local memory and a second one of the operands using a second relative position in the local memory, the first and second relative positions being contiguous with one another.

3. (Original) The method of Claim 2, wherein the first one of the operands and the second one of the operands comprise different numbers of bits.

4 - 5. (Canceled)

6. (Currently amended) A method of operating a cryptographic accelerator processor integrated circuit that comprises a local memory, the method comprising:

executing an instruction using the cryptographic accelerator processor that references at least one operand using a first relative position in the local memory, comprising:

generating a result based on the at least one operand; and

storing the result at a second relative position in the local memory;

wherein the first relative position comprises a first offset from a base address in the local memory, and the second relative position comprises a second offset from the base address in the local memory, and wherein the local memory is exclusively associated with the cryptographic accelerator processor.

7 - 15. (Canceled)

16. (Currently amended) A cryptographic data processing system that comprises a host processor, a system memory coupled to the host processor, and a cryptographic processor integrated circuit that comprises a local memory and is coupled to the host processor and the system memory, the system further comprising:

means for loading at least one operand from the system memory to the local memory; and

means for executing an instruction using the cryptographic processor that references the at least one operand using a first relative position in the local memory, comprising:

means for generating a result based on the at least one operand; and

means for storing the result at a second relative position in the local memory;

wherein the first relative position comprises a first offset from a base address in the local memory, and the second relative position comprises a second offset from the base address in the local memory; and

wherein the local memory is exclusively associated with the cryptographic processor.

17. (Original) The cryptographic data processing system of Claim 16, wherein the means for loading at least one operand from the system memory to the local memory

comprises means for loading at least two operands from the system memory to the local memory, and the means for executing the instruction comprises:

means for executing the instruction using the cryptographic processor that references a first one of the operands using the first relative position in the local memory and a second one of the operands using a second relative position in the local memory, the first and second relative positions being contiguous with one another.

18. (Original) The method of Claim 17, wherein the first one of the operands and the second one of the operands comprise different numbers of bits.

19 - 20. (Canceled)

21. (Currently amended) A cryptographic accelerator processor integrated circuit that comprises:

a local memory that is exclusively associated with the cryptographic accelerator processor; and

means for executing an instruction using the cryptographic accelerator processor that references at least one operand using a first relative position in the local memory, comprising:

means for generating a result based on the at least one operand; and

means for storing the result at a second relative position in the local memory;

wherein the first relative position comprises a first offset from a base address in the local memory, and the second relative position comprises a second offset from the base address in the local memory.

22 - 26. (Canceled)

27. (Currently amended) A computer program product for operating cryptographic data processing system that comprises a host processor, a system memory coupled to the host processor, and a cryptographic processor integrated circuit that comprises a local memory and is coupled to the host processor and the system memory, the computer program product comprising:

a computer readable program medium having computer readable program code embodied therein, the computer readable program code comprising:

computer readable program code for loading at least one operand from the system memory to the local memory; and

computer readable program code for executing an instruction using the cryptographic processor that references the at least one operand using a first relative position in the local memory, comprising:

computer readable program code for generating a result based on the at least one operand; and

computer readable program code for storing the result at a second relative position in the local memory;

wherein the first relative position comprises a first offset from a base address in the local memory, and the second relative position comprises a second offset from the base address in the local memory; and

wherein the local memory is exclusively associated with the cryptographic processor.

28. (Original) The computer program product of Claim 27, wherein the computer readable program code for loading at least one operand from the system memory to the local memory comprises computer readable program code for loading at least two operands from the system memory to the local memory, and the computer readable program code for executing the instruction comprises:

computer readable program code for executing the instruction using the cryptographic processor that references a first one of the operands using the first relative position in the local memory and a second one of the operands using a second relative position in the local memory, the first and second relative positions being contiguous with one another.

29. (Original) The computer program product of Claim 28, wherein the first one of the operands and the second one of the operands comprise different numbers of bits.

30 - 31. (Canceled)

32. (Currently amended) A computer program product for operating a cryptographic accelerator processor integrated circuit that comprises a local memory, the computer program product comprising:

a computer readable program medium having computer readable program code embodied therein, the computer readable program code comprising:

computer readable program code for executing an instruction using the cryptographic accelerator processor that references at least one operand using a first relative position in the local memory, comprising:

computer readable program code for generating a result based on the at least one operand; and

computer readable program code for storing the result at a second relative position in the local memory;

wherein the first relative position comprises a first offset from a base address in the local memory, and the second relative position comprises a second offset from the base address in the local memory, and wherein the local memory is exclusively associated with the cryptographic accelerator processor.

33 - 40. (Canceled)